Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1–20 (cancelled).

21. (Currently amended) A method for forming conducting structures separated by gaps on a substrate, comprising the steps of:

providing a substrate and a wiring layer above the substrate;

forming a cap layer above the wiring ~~line~~ layer;

forming a ~~first~~ mask layer above the cap layer;

etching the ~~first~~ mask layer to expose selected portions of the cap layer;

~~, and forming a second hard mask from a remaining portion of~~ etching the cap layer using the mask layer as a mask;

removing the mask layer to expose remaining portions of the cap layer;

etching the wiring ~~line~~ layer using the ~~second hard mask~~ remaining portions of the cap layer as a mask to form wiring lines separated by gaps, the wiring lines having ~~a~~ the remaining portion of the cap layer thereon, wherein the ~~first~~ mask layer is removed prior to the etching of the wiring ~~line~~ layer; and

depositing a dielectric material within the gaps at a sputtering rate sufficient to fill the gaps, using high density plasma chemical vapor deposition.

22. (Previously presented) The method of claim 21, wherein the cap layer comprises a material selected from the group consisting of a silicon nitride material and an oxynitride material.

23. (Previously presented) The method of claim 21, wherein a remaining portion of the cap layer on at least one wiring line has a rectangular shape in cross section.

24. (Previously presented) The method of claim 21, wherein a remaining portion of the cap layer on at least one wiring line has a trapezoidal shape in cross section.

25. (Previously presented) The method of claim 21, wherein the trapezoidal shape includes top and bottom surfaces parallel to one another and side surfaces that extend inwardly from the bottom surface to the top surface.

26. (Previously presented) The method of claim 21, wherein the remaining portion of the cap layer on at least one wiring line has a triangular shape in cross section.

27. (Previously Presented) The method of claim 21, wherein a remaining portion of the cap layer on at least one wiring line has, in cross section, a rectangular shape having its upper comers etched away.

28. (Previously presented) The method of claim 21, wherein a remaining portion of the cap layer is partially etched and redeposited into the gaps during the high density plasma chemical vapor deposition process.

29. (Previously presented) The method of claim 21, wherein a remaining portion of the cap layer is partially etched during the deposition of a dielectric material using high density plasma chemical vapor deposition.

30. (Currently Amended) The method of claim 21, wherein the ~~first~~ mask layer ~~is~~ comprises a patterned photoresist layer.

31. (Currently Amended) The method of claim 21, further comprising the formation of a surface layer between the substrate and the wiring ~~line~~ layer, the surface layer being a barrier between the substrate and wiring ~~line~~ layer.

32. (Currently Amended) The method of claim 21, wherein the cap layer comprises an oxide ~~second hard mask is substantially free of carbon compounds~~.

33. (Currently Amended) The method of claim 21, wherein the likelihood of contaminants being deposited within the gaps filled with the dielectric material is decreased by comparison to a process in which the mask layer is not removed prior to etching the wiring line ~~are substantially free of contaminants from the second hard mask~~.

34. (Previously Presented) The method of claim 33, wherein said contaminants include carbon compounds.

35. (Currently Amended) A method for forming conducting structures separated by gaps on a substrate, comprising the steps of:

providing a substrate and a wiring layer above the substrate;

forming a cap layer above the wiring ~~line~~ layer~~, wherein the cap layer is substantially free of carbon compounds~~;

forming a mask layer above the cap layer;

patterning the mask layer to expose selected portions of the cap layer;

etching the cap layer, and the wiring ~~line~~ layer, at the locations where the cap layer is exposed by the ~~etched~~ patterned mask layer, to form wiring lines separated by gaps without depositing contaminants from the mask layer in the gaps, the wiring lines having a remaining portion of the cap layer thereon; and

depositing a dielectric material within the gaps at a sputtering rate sufficient to fill the gaps, using high density plasma chemical vapor deposition.

36. (Currently Amended) The method of claim 35, wherein the mask layer is removed prior to the etching of the wiring ~~line~~ layer.

37. (Currently Amended) The method of claim 35, wherein the etched cap layer is used as a hard mask during the etching of the wiring ~~line~~ layer.

38. (Currently Amended) The method of claim 35, wherein ~~the~~ an amount of contaminant deposited in the gaps filled with the dielectric material is decreased by comparison to a process in which the mask layer is not removed

prior to etching the wiring line layer ~~are substantially free of contaminants from the mask layer~~.

39. (Previously Presented) The method of claim 38, wherein said contaminants include carbon compounds.

40. (Currently Amended) A method for forming conducting structures separated by gaps on a substrate, comprising the steps of:

providing a substrate and a wiring layer above the substrate;

forming a cap layer comprising nitride and/or silicon rich-oxide above the wiring ~~line~~ layer;

forming a mask layer above the cap layer;

etching the wiring ~~line~~ layer using the mask layer to form wiring lines separated by gaps, the wiring lines having a remaining portion of the cap layer thereon;

depositing a dielectric material within the gaps at a ~~sputtering rate~~ sufficiently high etch to deposition ratio to fill the gaps, using a high density plasma chemical vapor deposition (HDPCVD) process;

wherein the ~~high density plasma chemical vapor deposition (HDPCVD) process is performed with a sputtering rate which causes at least part of the~~ remaining portion of the cap layer protects ~~to be etched but without exposing~~ top corner sections of the wiring lines during the HDPCVD process ~~underlying the remaining portion of the cap layer~~.

41.(Previously Presented) The method of claim 40, wherein a facet is formed in the remaining portion of the cap layer during the HDPCVD process.

42.(Previously Presented) The method of claim 40, wherein the cap layer is formed with a facet adapted to reduce etching during the HDPCVD process.

43.(Previously Presented) The method of claim 40 wherein the cap layer comprises a material selected from the group consisting of a silicon nitride material and an oxynitride material.

44. (Currently Amended) The method of claim 40, wherein a sputtering rate of the HDPCVD process varies ~~is changed during~~ while the gaps are being filled with the dielectric material.